## REMARKS

Claims 1-4, 6-11, and 13-21 are all the claims pending in the application. Claims 5 and 12 are incorporated into independent claims 1 and 8, respectively and claims 5 and 12 are canceled, above. Claims 15-21 have been withdrawn from consideration pursuant to our previously filed Response to Restriction Requirement. Claims 1-4, 6-11, 13, and 14 stand rejected only on prior art grounds. Applicants respectfully traverse these objections/rejections based on the following discussion.

### I. The Prior Art Rejections

With respect to the prior art rejections, claims 1-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gardner et al, hereinafter "Gardner" (U.S. Patent No. 4,840,302) in view of Chang et al., hereinafter "Chang" (U.S. Patent No. 5,048,744) and Havemann (U.S. Patent No. 6,156,651).

**A. The 35 U.S.C. 103(a) Rejection Based on Gardner in view of Chang and Havemann.**

**1. The Position of the Office Action**

Regarding claims 1 and 2, the Office Action argues that Gardner discloses a metallurgical structure in an integrated circuit (IC) /chip having underlying circuitry/ components within an exterior covering comprising a passivation layer/exterior covering (cited in Gardner Col.4 in Fig. 1 and Col. 3) a via/hole (cited in Col. 3, line 26 Fig. 1) through the passivation layer extending to a metal line. The Office Action cites Col. 2 in Fig.1. Also, the Office Action asserts that Gardner discloses a barrier layer lining the via metal layers/plug (in Col. 12 in Fig. 1 and Col. 3, line 43). The Office Action further cites Gardner (Cols.14,16 and 18 in Fig. 1 and Col. 3, line 63) in the via above the barrier layer comprising copper, the metal line comprising copper (Col. 3, line 18), and a solder bump/connector (1 in Fig. 1; Col. 4, line 13) formed on the metal layers/plug (Fig. 1; Col. 2, line 64- Col, 4, line 31).

Regarding claim 3, the Office Action proposes that Gardner discloses the barrier layer comprising Ti and Cr but fail to specify the barrier layer comprising one or more layers of TiN, Ta and TaN. However, the Office Action offers that it is conventional in the chip packaging and interconnection technology art to use the materials such as Ti, Cr, Ta, TiN, etc. to improve the resistance against diffusion of

impurities and improve adhesion. The Office Action offers the admitted prior art (APA) specify using one or more layers of the materials such as Cr, W, Ti, etc. as a barrier layer. Therefore, the Office Action concludes it would have been obvious to the person of ordinary skill in the art at the time invention was made to incorporate the barrier layer comprising one or more layers of TiN, Ta and TaN to improve the resistance against diffusion of impurities in Gardner's structure as cited in claim 3.

Regarding claim 4, the Office Action recites that Gardner discloses using the barrier layer comprising Ti and Cr to improve the bond strength and reduce the contact resistance but fail to specify the use of the barrier layer to prevent the diffusion of elements within the solder bump into the metal line. However, the Office Action states use of barrier layers such as Ti, Cr, etc. to provide the diffusion barrier against elements/impurities from solder and to improve adhesion, bond strength and reliability of the interconnection/solder joint is well-known in the chip packaging and interconnection technology art. The Office Action cites prior art disclosed by Gardner Col. 1, line 51. Further, the Office Action claims that Chang teaches using Cr/Ti barrier layer to improve the diffusion/interaction and enhance conductivity between the solder and the metal such as copper. The Office Action refers to Col. 7, line 10; Col. 8, line 33; Figs. 8-11. Therefore, the Office Action resolves that it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the barrier layer to prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using

Chang's teaching in Gardner's structure as cited in claim 4.

Regarding claim 5, the Office Action renders that Gardner discloses forming a planar surface on the passivation layer exterior of the metallurgical structure comprising barrier layer, metal plug and solder ball as cited in Fig. 1; Col. 4, line 14. Regarding claim 6, the Office Action states Gardner discloses the solder ball being in direct contact with the metal plug (Fig. 1; Col. 4, line 5). Regarding claim 7, the Office Action states Gardner fails to specify a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball. However, the Office Action recites that Havemann teaches using conventional multilevel structure forming two levels of copper plugs/grooves with TIN barrier layer such that the second barrier layer is above the first metal plug and second metal plug is above the second barrier layer (Fig. 3G; Col, 4, line 55- Col. 5, line 38).

Therefore, the Office Action concludes it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second barrier layer above the metal plug and second metal plug above the second barrier layer with the second metal plug being in direct contact with the solder ball to further prevent the diffusion of elements within the solder bump into the metal line and to improve the reliability of the interconnection using Havemann's inter-connection structure in Gardner's structure as cited in claim 7. Further, the Office Action argues that the combined teachings of Gardner, Havemann and Chang apply to claims 8-13 as

explained above for claims 1-6 respectively.

**2. The Gardner Reference**

Gardner discloses an alloy for contacting portions of a conductive interconnect layer exposed by a overlying organic insulating layer having apertures therethrough. The alloy contains chromium and titanium, and is formed such that at least 50 nat % of the total content of the alloy is titanium at the alloy insulating layer Interface.

**3. The Change Reference**

Chang discloses the fluxless bonding in a reducing atmosphere of integrated circuit contacts containing copper is enhanced using a layer of 200 to 1500 Angstrom thick palladium which inhibits copper oxide formation before fusion and reduces all oxides to promote wetting during fusion.

**4. The Havemann Reference**

Havemann discloses a method of forming mechanically robust vias and entrenched conductors on a dielectric layer (which dielectric layer is on an electronic microcircuit substrate which vias and entrenched conductors are electrically connected

to a conductive area on the surface of the substrate) and a structure formed thereby. Generally some of the dielectric layers added above the microcircuit comprise a porous dielectric having a desirable low dielectric constant but low mechanical robustness. Special methods are described which generally comprise: forming the dielectric layer over the substrate; forming a nonporous dielectric layer over the substrate; depositing a planarizing stopping material over the top surface of said nonporous dielectric; depositing and patterning photoresist; etching said stopping material and nonporous dielectric layer in a conductor pattern to expose at least a portion of said conductive area on the surface of said substrate; depositing a wall seat depositing conductor metal; and planarizing said structure. Generally the via metal and the conductor metal consist essentially of aluminum, copper or combinations thereof. The conductor metal may be doped with the selectively deposited via metal being doped by dopant diffusion from the conductor metal, thereby avoiding the difficulty of depositing a doped selective metal. Methods are shown for realizing desirable insulating and conducting layers without deleterious mechanical effects.

## 5. Applicant's Response

In the claimed invention, the via is filled with a plug and planarized per Figures 2 and 3. This allows the passivation layer, barrier layer and plug to form a planar surface on which the solder ball rests. The prior art of record discloses

structures which do not fill the via and are not coplanar with the passivation surface. The unique claimed feature provides for a more robust barrier to tin migration and provides a better surface to deposit the Pb/Sn ball reducing manufacturing defects.

More specifically, independent claim 1 defines that the "metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure" and that the "solder bump formed on said planar exterior surface." Independent claim 8 defines a substantially similar feature.

To the contrary, the structure shown in Figure 1 of Gardner does not have a planar surface between the dielectric 4, the barrier layer 12 and the plug 14-18. Instead, Gardner has a contoured surface which generally follows the via to the underlying metal 2. Similarly, Chang does not disclose a barrier layer and plug that form a planar surface upon which the solder ball can connect. The only drawing in Chang which illustrate a via making contact with a lower metalization layer is Figure 11, and that Figure clearly shows a non-planar surface between the solder ball and the underlying layers.

Havemann is referred to as teaching copper plug/grooves within a barrier layer and is not referred to for teaching the claimed planar surface. Indeed, Havemann does not teach or suggest the claimed structure which provides a planar surface upon which to mount the solder ball.

In view of the foregoing, Applicants respectfully submit that the invention as defined by independent claims 1 and 8 is not taught or suggested in the prior art of

record. Therefore, independent claims 1 and 8 are patentable over the prior art of record. Further, dependent claims 2-4, 6, 7, 9-11, 13, and 14 are similarly patentable, not only by virtue of their dependency from a patentable independent claim, but also by virtue of the additional features of the invention they define.

In view of the foregoing, Applicants submit that claims 1-4, 6-11, 13, and 14, all the claims presently being examined in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any over payments to Attorney's deposit account number 09-0456.

Respectfully submitted,

Dated: 5/29/01

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**Attachment**

**Marked Up Version of Changes Made**

1. (Amended) A metallurgical structure comprising:

a passivation layer;

a via through said passivation layer extending to a metal line within said metallurgical structure;

a barrier layer lining said via;

a metal plug in said via above said barrier layer, [said metal plug and said metal line comprising a same material] wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure; and

a solder bump formed on said [metal plug] planar exterior surface.

**Please cancel claim 5 without prejudice or disclaimer.**

8. (Amended) An integrated circuit structure comprising:

internal components within an exterior covering;

a via extending through said exterior covering to said internal components;

a barrier layer lining said via;

a plug in said via above said barrier layer, [said plug and said internal components comprising a same material] wherein said plug and said barrier layer form a planar exterior surface of said integrated circuit structure; and

8 a connector formed on said [plug] planar exterior surface.

**Please cancel claim 12 without prejudice or disclaimer.**